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The Control Of Oxygen Precipitation And The Impact Of Internal Gettering

Vacancy concentration profiles result in ideal precipitation for gettering.

- Controlling oxygen behavior in silicon wafers via vacancy profiles is more cost-effective than conventional out-diffusion and renucleation methods.
- Proper vacancy programming forces the wafer to behave in a specific way.
- The vacancy-based approach greatly simplifies the use of silicon by decoupling the formation of the IG structure from the details of the thermal process used in device fabrication.

Controlling oxygen behavior in silicon is undeniably one of the most important challenges in semiconductor materials engineering. In particular, control of oxygen precipitation is essential for the development of internal gettering (IG) in IC manufacturing. Gettering schemes play an important role in yield management in IC manufacturing. In the 20 or so years since the discovery of the IG effect in silicon wafers, many scientists and engineers have struggled with the problem of precisely and reliably controlling the precipitation of oxygen that occurs in silicon during the processing of wafers into integrated circuits. This has met with only partial success, in the sense that the "defect engineering" of conventional silicon wafers is still an empirical exercise. It consists largely of careful, empirical tailoring of wafer type (oxygen concentration, crystal-growth method, and details of any additional preheat treatments, for example) to match the specific process details of the application to which the wafers are submitted, in order to achieve good and reliable IG performance.

Reliable and efficient IG requires the robust formation of oxygen-precipitate-free surface regions ("denuded zones") and a bulk defective layer consisting of a minimum density1 (at least about $10^8 cm^{-3}$) of oxygen precipitates during the processing of the silicon wafer. Uncontrolled precipitation of oxygen in the near-surface region of the wafer represents a risk to device yield. The basis of the conventional method for dealing with the creation of this layered structure has been to ensure sufficient outdiffusion of oxygen from the near-surface region in order to suppress nucleation and growth. In recent years, due to radical reductions in the total thermal budgets of processes that make submicron devices, this method is no longer cost-effective.

It is possible to install vacancy-concentration profiles into silicon wafers that result in the ideal precipitation performance for IG purposes. Such an ideal vacancy profile means a high vacancy concentration in the wafer bulk and proper vacancy depletion in the near-surface region. The installation of controlled concentration profiles of vacancies is now a wafer-manufacturing process, as depicted in Figure 1. While a high concentration of vacancies enhances oxygen clustering, there is a lower bound on vacancy concentration below which clustering is "normal". This is quite a sharp transition and lies around $5X10^{11} cm^{-3}$. Thus a profiled vacancy concentration allows for the programming of "layered" structures — exactly what is required for the effective engineering of structures by IG. This is the basis underlying the "Magic Denuded Zone" (or MDZ) wafer.[2] A schematic illustration of this new materials-processing technique is shown in Figure 2. The use of such a vacancy-based approach greatly simplifies the use of silicon by decoupling the formation of the IG structure from the details of the crystalgrowth process, the oxygen content of the wafer, and the details of the thermal process used to fabricate the device in question.

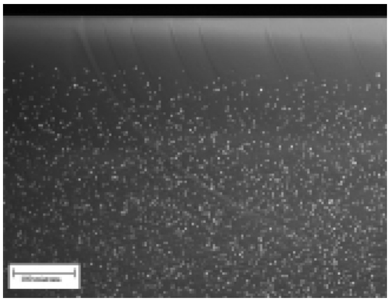

Figure 1: *An etched cross-section of a silicon wafer with an ideal distribution of oxygen precipitates for internal gettering.*

The Installation of Vacancy-Concentration Profiles in Silicon Wafers

The installation of appropriate vacancyconcentration profiles in silicon wafers is a nthree-step process, but all steps occur in a single rapid thermal processing (RTP) run.[2]

1. When silicon is raised to high temperatures, vacancies and interstitials are spontaneously produced in equal

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amounts through Frenkel pair generation, a very fast reaction. At distances far removed from crystal surfaces, we thus have $C_I = C_V = \{C_I^{eq}(T)C_V^{eq}(T)\}^{1/2}$, where T is the process temperature. If the sample were to be cooled at this point, the vacancies and interstitials would mutually annihilate each other in the reverse process of their generation.

2. In wafers, however, the surfaces are not far away, and this situation changes very rapidly. Equilibrium boundary conditions (not oxidizing or nitriding) lead to coupled fluxes of interstitials to the surface and vacancies from the surface because $C_I^{eq}(T) < C_V^{eq}(T)$, and because of the rapid establishment of equilibrium conditions throughout the thickness of the wafer. Experiments suggest that this occurs in a matter of seconds or less. This equilibration

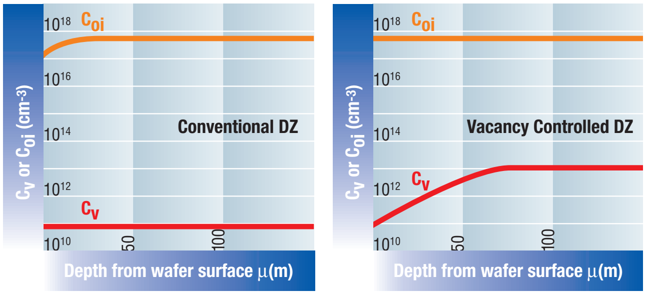

Figure 2: *A schematic illustration of the difference between conventional methods of installing denuded zones in silicon wafers via oxygen out-diffusion and renucleation and MDZ® based on the installation of tailored vacancy concentration profiles.*

is primarily controlled by the diffusivity of the fastest component, the self-interstitials, since the concentrations are roughly equal.

3. Upon cooling, two processes are important: direct recombination of vacancies and interstitials, and diffusion of interstitials toward the surfaces. In the wafer bulk, the slower vacancies are now the dominant species of the coupled diffusion, and hence the equilibration process at the surface is not as fast as the interstitial-dominated initial equilibration. It is thus possible to “freeze-in” excess bulk vacancies at not-unreasonable cooling rates (ca. 50-100°C/s). The residual bulk concentration of vacancies following recombination with interstitials, C_V, is the initial difference of $C_V^{eq} - C_I^{eq}$ (at the process temperature T). Closer to the surfaces, C_V is lower, due to out-diffusion (again, primarily controlled by the dominant vacancies) toward the decreasing equilibrium values at the wafer surface. The level of bulk precipitation is controlled by the process temperature, through $C_V^{eq} - C_I^{eq}$, while the depth of the denuded zone is controlled by the cooling rate, through the diffusion of vacancies during cooling.

By installing a given precipitate profile into a silicon wafer, we have effectively *programmed* it to behave in a certain way. The precipitate profiles that result from the vacancy-programming such as is illustrated in Figure 2 produce perfect internal gettering performance reliably and reproducibly.

The denuded, or oxygen precipitate free, zone in MDZ® is a real one in the sense that the near surface density of oxygen precipitates is effectively zero. In other approaches to the problem this is not necessarily the case. For example, when oxygen precipitation enhancement is attempted at the crystal growth level, as in the case of nitrogen-doped silicon, no “real” denuded zones are possible. The high temperature oxygen out-diffusion treatments which are applied to such wafers result in an “apparent” denuded zone only. The grown-in precipitates are not themselves dissolved. The oxygen concentration reduction near the surface merely restricts the size of precipitates there; at some point they cannot be detected by simple etching. But the density of oxygen related defects, in fact, remains the same — all the way to the wafer surface. Crystal-growth based precipitation enhancement schemes increase the constraints placed on the crystal growth process. MDZ® frees the crystal growth process to be whatever it needs to be to decrease costs.

The precipitate structure is dictated by the vacancy concentration profile installed in the wafer. Proper vacancy programming forces the wafer to behave in an ideal way. It does not matter what the oxygen content of the wafer is. It does not matter what the crystal growth process was that produced the wafer — the MDZ® process erases the crystal-history of the wafer. From an IC manufacturer’s point of view, a single, highly simplified specification can now cover a multitude of applications and product ranges, hugely simplifying their use and increasing flexibility. ■

References:

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