MEMC
TECHNOLOGY IS BUILT ON US

Advanced COP-Free Silicon Substrate For Next Generation IC Devices:

Optia™

Improve Device Performance, Reliability, and Cost of Ownership

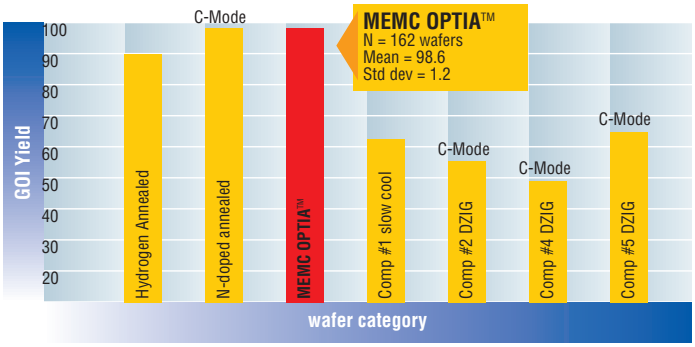
- No harmful crystal defects in the surface and bulk leads to no crystal defect-related yield and reliability degradation
- Better quality, performance and cost of ownership than annealed wafers
- Deep precipitate-free zone through MDZ® maintained throughout customer processing leads to improved device yield and reliability potential
- Built-in IG template through MDZ® eliminates need for customer oxygen out-diffusion and nucleation and reduces customer cycle time

The OPTIA™ wafer is a high performance silicon substrate for the VLSI and ULSI IC device generations. These devices are built today with increasingly denser and more complex architectures. Consequently, increasingly tighter specifications are required for silicon substrates.

Crystal-related defects in the wafers have been correlated with decreased GOI (gate oxide integrity) performance. OPTIA™ wafers have zero crystal-originated pits (COPs) and epi-like GOI, therefore, they provide an ideal solution for next generation IC devices.

OPTIA™ wafers are free of agglomerated defects across the wafer and throughout the whole wafer thickness. OPTIA™ wafers are enhanced using MEMC's patented Magic Denuded Zone® (MDZ®) thermal treatment. MDZ® produces a deep precipitate free zone and provides robust internal gettering protection early in the IC fabrication process.

200mm OPTIA™ GOI performance vs. competitors wafers



(Source: MEMC AE benchmarking, 2000)

Vacancy-related defects and GOI performance

Agglomerated vacancy-related defects are known commonly as D-defects, or as COPs when they intersect the wafer surface. Although recent data has shown a decreasing sensitivity of GOI to COPs at gate oxide thickness of less than 100Å, it is believed that the presence of the vacancy-related defects will have a certain impact on device performance and yield.

The benefits of OPTIA™ wafers arise because of the complete suppression of agglomerated defects, which lead to COPs and interstitial defects. Therefore, the device yield and reliability potential are improved by the use of OPTIA™ wafers.

LPDs:
- **30 max @ > 0.12 micron for 200mm**
- **50 max @ > 0.12 micron for 150mm**

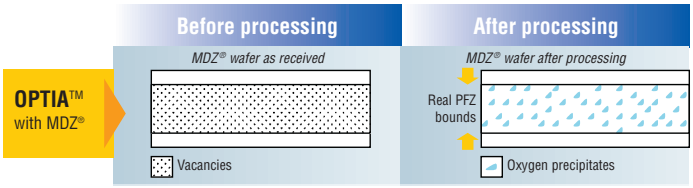
GOI:
> 95% for 150mm and 200mm

Advanced Flatness:
SFQR ≤ 0.2µm for 200mm

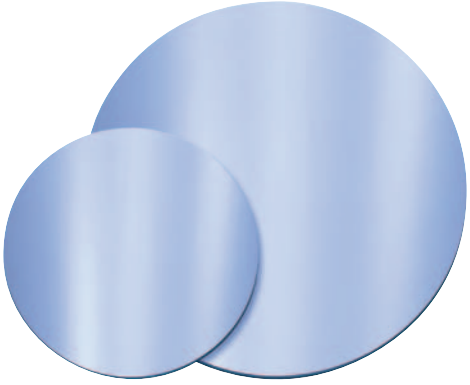
Intrinsic gettering

In addition to low COP densities, many customers also require intrinsic gettering. This is achieved in OPTIA™ wafers by using MEMC's patented process Magic Denuded Zone® (MDZ®). The MDZ® process produces an ideal density of oxygen precipitates and a deep precipitate-free zone. This eliminates the need for additional, costly out-diffusion, nucleation and growth thermal cycles in the customers' manufacturing lines.

The MDZ® Advantage



MDZ® installs in the OPTIA™ wafer the right precipitate depth distribution, at the wafer level.



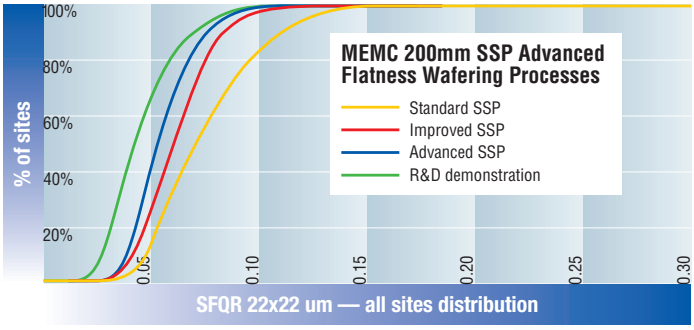
Available in 200mm and 300mm

	Standard	Slow cool	Advanta™	Annealed	Optia™	CMOS Epi (p/p+) or AEGIS™
Wafer Type	Open HZ	Vancancy-rich, no V/I boundary	Vacancy core, no V/I boundary	Low-COP, no V/I boundary	Zero COP, no V/I boundary	Zero COP, no V/I boundary
# LPDs ≥ 0.12 µm	500 max	400 max	200mm 50 max 150mm 80 max	30 max	200mm 30 max 150mm 50 max	30 max
FPD Void Density (cm^2)	300	100	200, only in core	100's (0-10 µm under surface)	0	0
GOI Yield, 200A, 10V/cm(%)	30-70	50-80	65-85	≥ 95	≥ 95	≥ 95
COP-free zone depth (µm)	0	0	Entire wafer in outer ring, 0 in core	10	Entire wafer	Epi thickness

Flatness performance

OPTIA™ is manufactured using MEMC's newest wafering technology processes, which can produce flat, super-flat, and ultra-flat wafers, as required by current and next-generation IC devices.

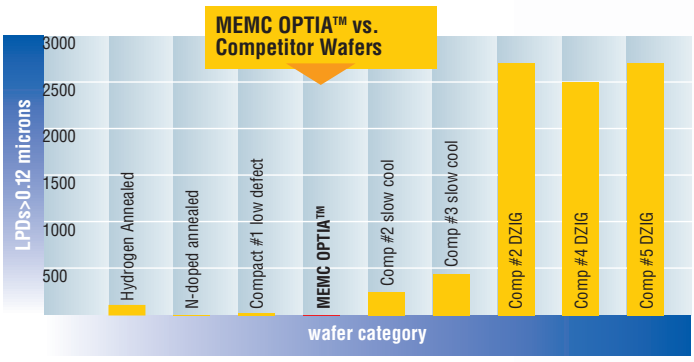
MEMC 200 mm SSP Advanced Flatness Wafering Processes



OPTIA™ characteristics

The OPTIA™ wafer is an extremely reliable material for the sub-0.18 µm generation IC devices, offered at great cost of ownership effectiveness compared to other high performance wafers available on the market.

200mm OPTIA™ LPD performance vs. competitive wafers



(Source: MEMC AE benchmarking, 2000)

Optia™

OPTIA™ SILICON WAFERS COMBINE TWO PROVEN SOLUTIONS IN ONE WAFER:

Perfect Silicon™

Silicon that's defect-free throughout the thickness of the entire wafer

MDZ® MAGIC DENUDED ZONE BY MEMC

A drop-in solution that provides a deep precipitate-free zone with robust intrinsic gettering.

THAT'S A RECIPE FOR SURVIVING BELOW 90NM.

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Optia™

The OPTIA™ Advantage

- OPTIA™ is a long-term silicon solution that delivers yield and device performance as you transition to advanced device processes.
- OPTIA™ is an easy to specify product that will perform well across your entire range of device technologies.
- OPTIA™ provides you with the opportunity to improve your total cost of ownership through the elimination of furnace steps early in the fab process.

OPTIA™ provides a number of proven solutions to problems typically encountered in device manufacturing and end user performance:

Problem	Solution	Result
Yield loss due to gate oxide integrity (GOI) issues.	MDZ® rapid thermal process technology in which the oxygen precipitation behavior is controlled by manipulation of vacancy rather than oxygen concentration profiles.	Improvements in yields up to 10%.
Increased processing costs due to long thermal treatments.	OPTIA™ wafers do not rely on long thermal treatments in the IC fab process.	Reduction in thermal budgets up to 40%
Device loss due to metal contamination.	OPTIA™ p will effectively getter high levels of metals such as Copper, Nickel, and Iron.	Improvement in device reliability.
Crystal defect related yield and reliability degradation.	Elimination of harmful crystal defects in the surface and bulk.	No crystal defect related yields or reliability degradation.

MEMC®

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